A 155-GHz Monolithic Low-Noise Amplifier

Huei Wang, *Senior Member, IEEE,* Richard Lai, Yon-Lin Kok, Tian-Wei Huang, Michael V. Aust, Yaochung C. Chen, *Member, IEEE,* Peter H. Siegel, *Senior Member, IEEE,* Todd Gaier, Robert J. Dengler, and Barry R. Allen, *Member, IEEE*

***Abstract*— This paper presents the design, fabrication, and test results of a three-stage 155-GHz monolithic low-noise amplifier (LNA) fabricated with the 0.1-μm pseudomorphic (PM) InAlAs/InGaAs/InP HEMT technology. With this amplifier in a test fixture, a small-signal gain of 12 dB was measured at 155 GHz, and more than 10-dB gain from 151 to 156 GHz. When the amplifier was biased for a low noise figure (NF), an NF of 5.1 dB with an associated gain of 10.1 dB was achieved at 155 GHz. All the results above are referred to the monolithic-microwave integrated-circuit (MMIC) chip with the input and output waveguide-to-microstrip-line transition losses corrected.**

***Index Terms*—InP, LNA, MMIC, pHEMT.**

I. Introduction

MILLIMETER-WAVE (MMW) low-noise amplifiers (LNA's) are very important components for smart munitions, passive imaging, and radiometer applications. The pseudomorphic (PM) high electron-mobility transistor (HEMT) devices with both GaAs and InP materials have demonstrated the high-gain and low-noise capability at W-band (75–110 GHz) and D-band (110–170 GHz) frequencies for hybrid integrated circuits [1]–[2]. High-gain LNA's have been successfully developed up to 140 GHz [3]–[6], as referred in the summary of previously published InP-based HEMT MMIC LNA results listed in [12]. For the frequency range above 120 GHz, InP-based HEMT's are superior to GaAs-based HEMT's for amplification due to the higher electron peak-drift velocity in the InP-based HEMT devices. The MMIC LNA's fabricated with the InP HEMT monolithic-microwave integrated-circuit (MMIC) process have also achieved high gain and low noise-figure performance at lower frequencies. Examples include a Q-band (44.5 GHz) two-stage balanced LNA exhibiting 2.2-dB noise figure (NF) with 20-dB associated gain [7], and a W-band four-stage balanced amplifier with a small-signal gain of 23 dB from 75 to 110 GHz [8]. A two-stage cryogenically cooled W-band LNA also exhibited 0.7-dB NF at 95 GHz with 12-dB associated gain [9]. The motivation of this paper was to push the state-of-the-art by demonstrating higher frequency performance in a monolithic LNA using the 0.1-μm passivated InP-based HEMT MMIC technology [11].

This paper describes the design, fabrication, and testing of a 155-GHz monolithic three-stage amplifier fabricated with the 0.1-μm InAlAs/InGaAs/InP PM HEMT technology. A small-signal gain of 12 dB was achieved at 155 GHz for the MMIC chip. When this MMIC is biased for low NF, 5.1-dB NF with 10.1-dB associated gain was obtained. This is the highest frequency amplifier ever reported to date using three terminal devices and defines the state-of-the-art of InP HEMT MMIC LNA's.

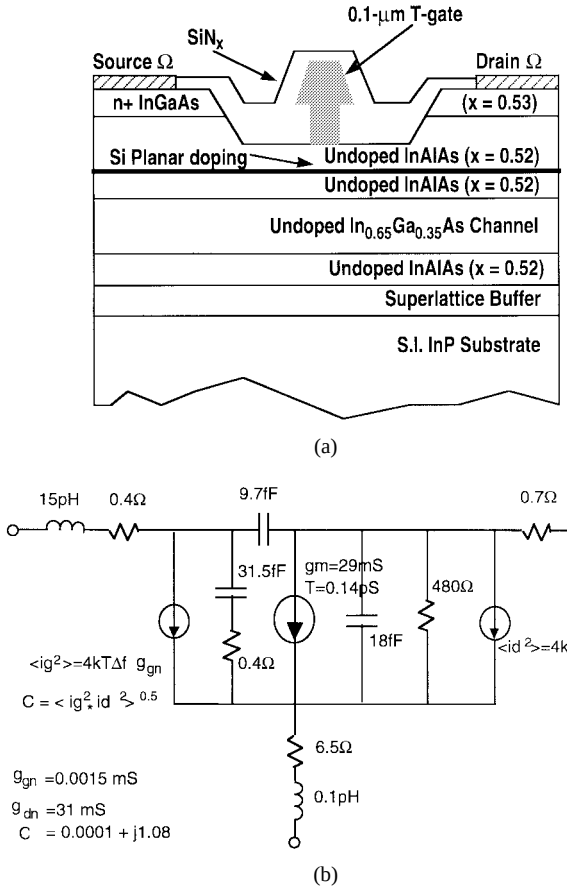


Fig. 1. (a) InGaAs/InAlAs/InP PM HEMT device layer structure. (b) The four-finger 30-μm HEMT device small-signal equivalent-circuit and noise model at 0.9-V drain bias with a drain current of 8 mA.

II. Device Fabrication and Characteristics

The three-stage 155-GHz MMIC LNA chip was fabricated on a 2-in Fe-doped semi-insulating InP substrate grown

Manuscript received October 11, 1997; revised July 21, 1998.

H. Wang was with the Space and Electronics Group, TRW, Redondo Beach, CA 90278 USA. He is now with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, R.O.C.

R. Lai, Y.-L. Kok, M. V. Aust, Y. C. Chen, and B. R. Allen are with the Space and Electronics Group, TRW, Redondo Beach, CA 90278 USA.

T.-W. Huang was with the Space and Electronics Group, TRW, Redondo Beach, CA 90278 USA. He is now with the Wireless Broadband Network Division, Lucent Technologies, Milpitas, CA 95035 USA.

P. H. Siegel, T. Gaier, and R. J. Dengler are with the Jet Propulsion Laboratory, Pasadena, CA 91109 USA (e-mail: gaier@merlin.jpl.nasa.gov).

Publisher Item Identifier S 0018-9480(98)08026-0.

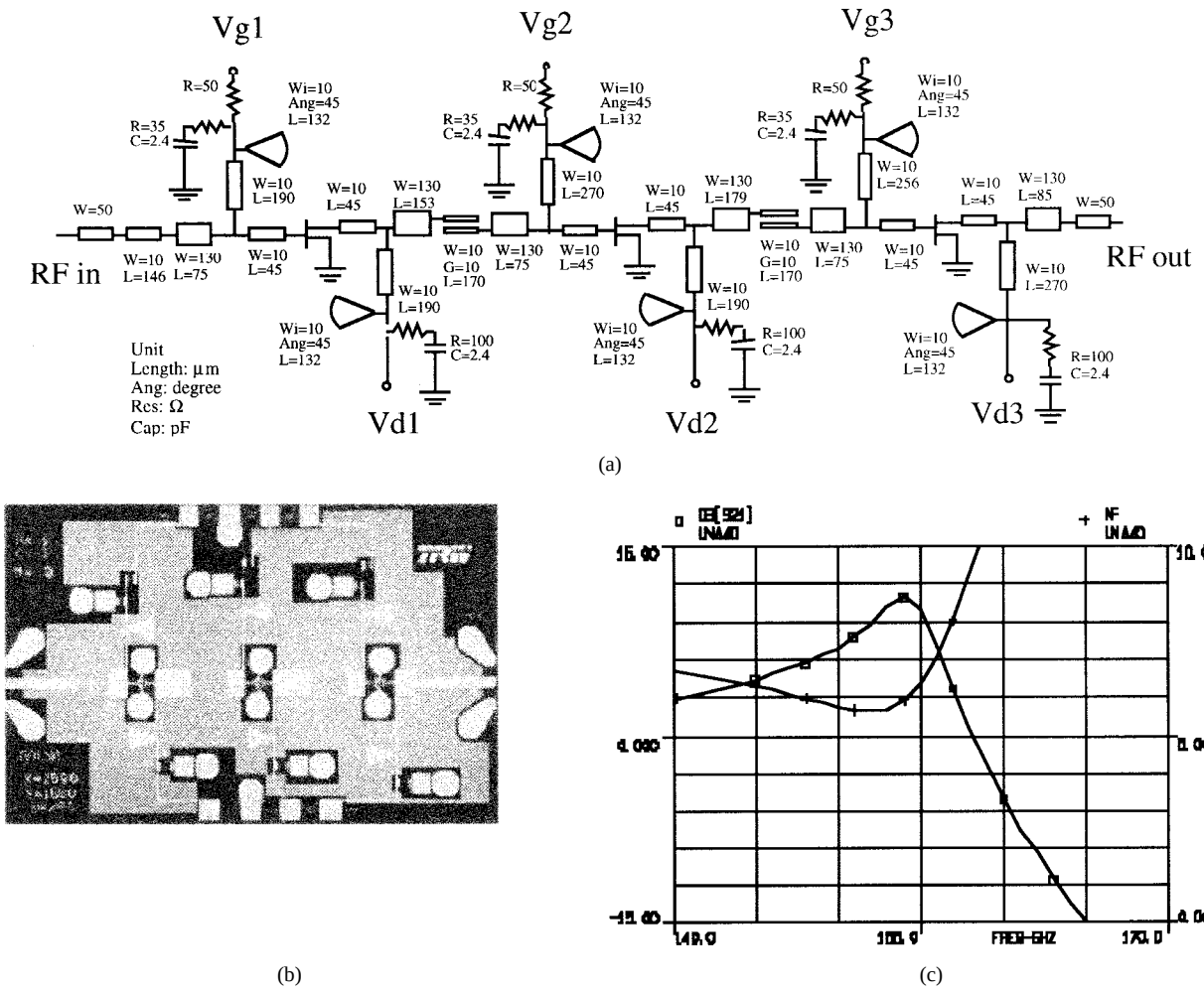


Fig. 2. (a) Circuit schematic diagram. (b) Chip photograph (chip size: 2.5 mm× 1.6 mm). (c) The simulated small-signal gain and NF from 140 to 170 GHz of the 155-GHz InP-based HEMT MMIC LNA.

by molecular beam epitaxy (MBE) and employs 0.1-μm T-gate InP HEMT devices. The InAlAs/InGaAs/InP HEMT ($In_{0.65}Ga_{0.35}As$ channel) structure InP HEMT MMIC process follows the procedures reported in [2], with additional wafer passivation and stabilization bake steps introduced to the MMIC process [11]. Fig. 1(a) shows the InP HEMT device layer structure. The channel is a 150 Å PM 65% Indium composition InGaAs layer, which provides superior transport properties and high electron sheet densities. Typical room-temperature Hall mobility of 10500–11 000 cm^2/V-s and Hall sheet carrier concentration of 3.5×10^{12}/cm^2 were measured on undoped-cap layer-calibration samples.

The devices are isolated using a combination of a wet etch/boron implantation process, which provides better than 10 MΩ/□ resistance. Source and drain Ni/Au-Ge/Ag/Au ohmic contacts alloyed at 400 °C using rapid thermal annealing, provide a very low ohmic contact resistance of 0.06 Ω · mm and a source resistance of 0.2 Ω · mm. The 0.1-μm gate strips are fabricated with a bi-layer PMMA/PMMA-MAA resist profile for metal liftoff and are offset by 0.6 μm from the source pad. Prior to metallization, the devices are gate recess etched to a predetermined current level. The target device pinchoff voltage of −0.25 V with the voltage at a

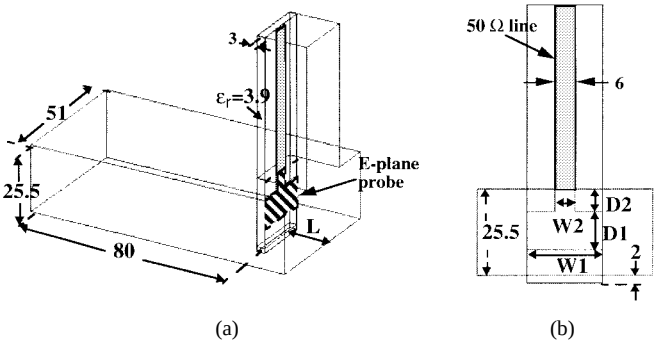
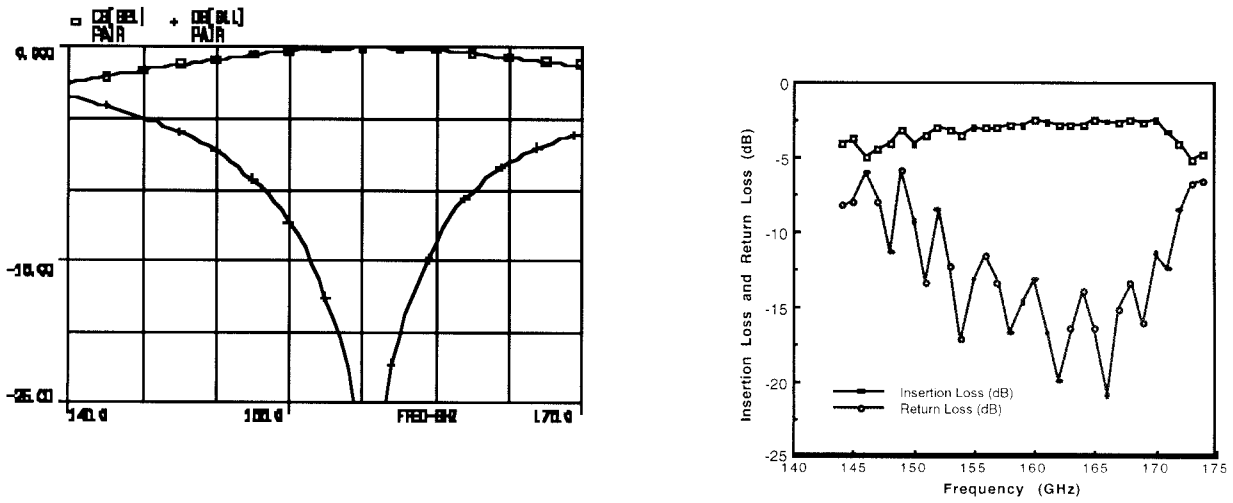


Fig. 3. (a) Three-dimensional view of the waveguide-to-microstrip-line transition, all dimensions are in mil (0.001 in). (b) Top view of the microstrip line, $D1 = 0.011$in, $W1 = 0.03$in, $D2 = 0.007$in, $W2 = 0.006$in, $L = 0.0185$in.

peak transconductance (V_{gp}) of 1000 mS/mm, are attained with a unity current gain frequency (f_T) of 200 GHz, and a maximum oscillation frequency (f_{max}) of 400 GHz. Device reverse-breakdown voltage, defined at 0.2 and 1.0 mA/mm reverse gate–leakage current are 1.5 and 2.5 V, respectively. The devices are passivated with 750-Å silicon nitride deposited using PECVD. For the MMIC process, precision NiCr resistors with a target resistance of 100 Ω/□ and



(a) (b)

Fig. 4. (a) Simulated and (b) measured through insertion loss and return loss of a pair of back-to-back transitions between 140 and 175 GHz.

silicon–nitride metal–insulator–metal (MIM) capacitors with a target sheet capacitance of 300 pF/mm^2 are used. After processing the frontside, the wafers are lapped and polished to 75-μm thickness. Ground via holes are wet-chemical etched and 3.5-μm gold is plated on the back side of the wafers to complete the MMIC process.

III. Device Modeling and Circuit Design

The linear small-signal model for a 0.1-μm gate PM InP HEMT used in this 155-GHz LNA design was obtained from curve fitting of the measured transistor small-signal S-parameters up to 50 GHz. The resulting equivalent-circuit parameters are consistent with the estimated values based on device physical dimensions and electrical/process parameters. The four-finger 30-μm-device small-signal equivalent-circuit model and the noise model at 0.9-V drain voltage with 8-mA drain current are shown in Fig. 1(b).

Fig. 2(a) shows the schematic diagram of this monolithic amplifier, and Fig. 2(b) shows the chip photograph with the chip size of 2.5 mm $\times$ 1.6 mm. The 155-GHz amplifier is a three-stage single-ended design. Each stage uses a four-gate finger 30-μm PM InP HEMT device for low gate resistance and gate–drain capacitance for have high device gain at the frequency. As can be obtained from the device model in Fig. 1(b), the optimal noise reflection coefficient ($\Gamma_{\rm opt}$), normalized noise resistance (R_n), and input reflection coefficients (S_{11}) in the common source configuration with source inductance from the two parallel grounding via holes (around 20 pH each, 10 pH total) at 155 GHz are $0.642\angle 175°$, 0.088, and $0.642\angle -173°$, respectively. The calculated minimum NF $(\mathrm{NF}_{\min})$ is 2.8 dB at 155 GHz. The circuit design utilizes a quasi-low-pass topology in the matching structures similar to that used in the previously published 140-GHz MMIC LNA [6]. This simple matching topology was chosen to minimize the uncertainties in the analysis and modeling at such a high frequency and, thus, reduce the design risk. The input, output, and inter-stage matching networks are all constructed by cascading high–low impedance microstrip lines on a 75-μm-thick InP substrate. Edge-coupled lines are used for dc blocking and radial stubs are employed for RF bypass. Shunt *RC* networks are included in the bias circuitry to maintain amplifier stability. A wet chemical-etching process is used to fabricate the backside via holes for grounding. The design and analysis procedures of the monolithic chip design, which include accurate active device modeling and full-wave electromagnetic (EM) analysis of passive structures (SONNET software) are documented in [10]. The simulated small-signal gain and NF are plotted from 140 to 170 GHz in Fig. 2(c). It shows a peak gain of 11 dB at 154 GHz with an NF of 5.9 dB.

IV. Transition and Test-Fixture Design

For testing, the InP amplifier chip is coupled to WR-5 waveguide at the input and output through a quartz E-plane probe structure. The probe was designed by utilizing a waveguide-to-microstrip cross-junction structure, similar to the designs used at lower frequencies (26–110 GHz) [13]. The full-wave EM analysis software package HFSS[1] was used for the design. A schematic is shown in Fig. 3 along with transition dimensions. The transition consists of a printed microstrip-line circuit on 0.003-in-thick fused quartz, a portion of which extends into the WR5 (140–220 GHz) waveguide through an aperture in the broad wall. The width of the quartz substrate is chosen to eliminate waveguide modes in the microstrip cavity. In order to have a low insertion loss and to be insensitive to mechanical alignment error between the probe and waveguide, the probe sectional lengths ($D1$ and $D2$), widths ($W1$ and $W2$), and the back-short location (L) are designed to have relatively large values. The dimensions of the transition are given in the figure caption. The simulated insertion loss and return loss of a pair of back-to-back transitions are plotted in Fig. 4(a).

For determining the transition loss and match, two fixtures were connected back-to-back with a 0.130-in-long 0.006-in-wide microstrip line joining the waveguide. The measured fre-

[1] HFSS, *HP 85180A High-Frequency Structure Simulator User's Reference*, Hewlett-Packard Company, Network Measurement Division, Santa Rosa, CA 95403.

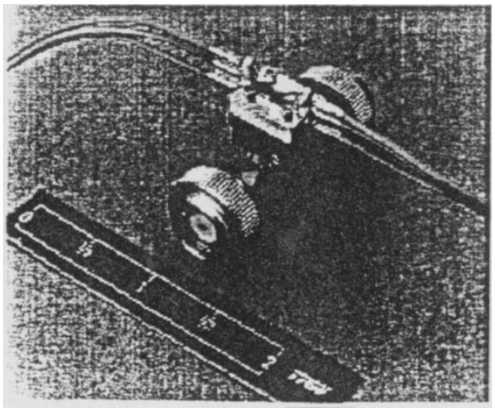


Fig. 5. Photograph of the 155-GHz MMIC LNA mounted in the transition test fixture.

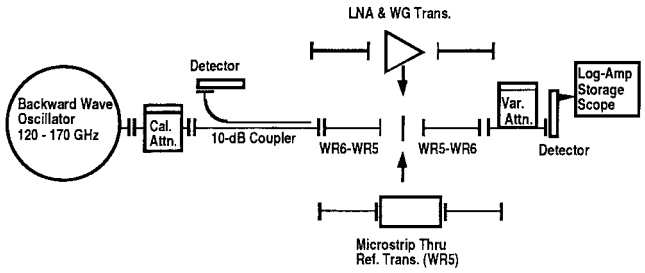


Fig. 6. Block diagram of the scalar test system for measuring amplifier gain. The calibrated attenuator is used to set the reference gain levels. The variable attenuator is used for detector matching. All unlabeled waveguide is WR6 (110–170 GHz).

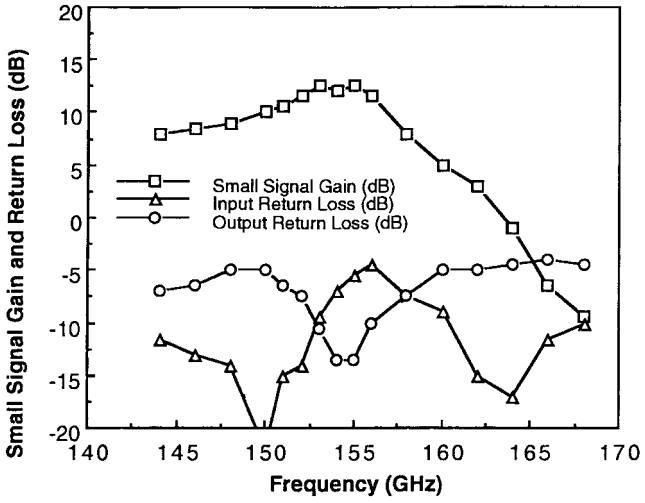


Fig. 7. Measured small-signal gain (referred to the chip) and return loss of the 155-GHz MMIC LNA from 144 to 170 GHz ($V_d = 1.4$ V, $I_{\rm total} = 25$ mA).

quency response from 144 to 170 GHz is shown in Fig. 4(b). The insertion loss for a pair of back-to-back transitions is approximately 2.5 dB and the return loss is about 15 dB from 152 to 168 GHz. The simulated insertion loss is very low since lossless metal and materials are assumed to save computation time. However, the optimal return loss is predicted to be at about the right frequency. It is noted that in the real waveguide assembly, especially at this frequency, there are a number

TABLE I
AMPLIFIER GAIN AND OUTPUT POWER OF THREE INPUT POWER LEVELS (REFERRED TO THE CHIP) AT 155 GHz ($V_d = 1.4$ V, $I_{\rm total} = 25$ mA)

Input Power (dBm)	Power Gain (dB)	Output Power (dBm)
-18.75	12	-6.75
-13.75	12	-1.75
-8.75	10.5	1.75

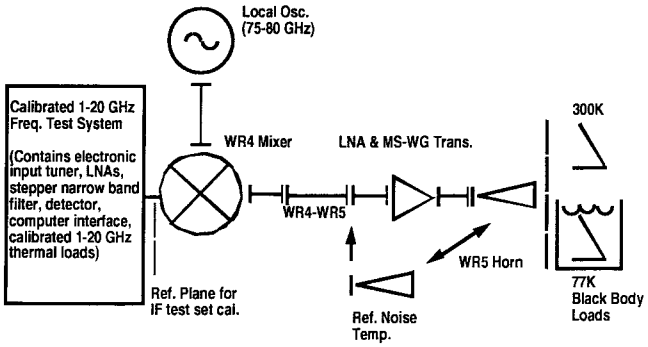


Fig. 8. Block diagram of the noise measurement test setup.

TABLE II
MEASURED NOISE FIGURE AND ASSOCIATED GAIN AT 150, 155, AND 160 GHz AT HIGH-GAIN BIAS CONDITION ($V_d = 1.4$ V, $I_{d1,2,3} = 10$ mA). THE NUMBERS IN THE PARENTHESIS ARE ESTIMATED CHIP PERFORMANCE ACCOUNTING THE 2.5-dB TRANSITION LOSS (2.5 dB ADDED FOR GAIN AND 1.25 dB SUBTRACTED FOR NF)

Frequency (GHz)	Noise Figure (dB)	Associated Gain (dB)
150	7.9 (6.6)	6.6 (8.1)
155	8.1 (6.8)	8.5 (11)
160	8.3 (7.1)	4.4 (6.9)

of items which cannot be ideal, such as the E-plane probe alignment, substrate material fabrication tolerance, etc. All these contribute to the discrepancy from theory to experiment.

V. AMPLIFIER MEASUREMENT

The 155-GHz LNA chip was mounted and tested in the G-band (WR5, 140–220 GHz) waveguide fixture described in Section IV. A photograph of the complete fixture with the MMIC chip mounted is shown in Fig. 5. The amplifier gain and return losses were measured with a scalar-network-analyzer test system based around a 120–170-GHz backward-wave oscillator. A block diagram of the measurement setup is shown in Fig. 6. A series of reference sweeps were taken using a calibrated attenuator, and device-under-test (DUT) was inserted in order to measure the amplifier gain and fixture insertion loss. Fig. 7 shows the gain and input/output return loss from 144 to 170 GHz. A peak gain of 12 dB occurs between 153–155 GHz and the amplifier demonstrates more than 10-dB gain from 151 to 156 GHz. The input and output return losses are better than 5 and 10 dB, respectively. The gain curve refers to the chip, which has had 2.5 dB added to account for the transition loss. The total dc power consumption is only 35 mW ($V_d = 1.4$ V, $I_{\rm total} = 25$ mA). The gain

TABLE III
MEASURED NF AND ASSOCIATED GAIN THROUGH THE AMPLIFIER AND WAVEGUIDE TEST FIXTURE OF THE 155-GHz LNA AS A FUNCTION OF DRAIN CURRENT IN EACH STAGE (DRAIN VOLTAGE FIXED AT 1.4 V). THE NUMBERS IN THE PARENTHESIS ARE ESTIMATED CHIP PERFORMANCE ACCOUNTING THE 2.5-dB TRANSITION LOSS (2.5 dB ADDED FOR GAIN AND 1.25 dB SUBTRACTED FOR NOISE FIGURE)

I_{d1}(mA)	I_{d2}(mA)	I_{d3}(mA)	NF (dB)	Gain (dB)
5	10	10	7.9 (6.6)	8.0 (10.5)
5	7	10	7.5 (6.3)	8.0 (10.5)
5	7.3	7.1	7.3 (6.1)	7.9 (10.4)
3	7.3	7.1	7.2 (5.9)	7.5 (10.0)
3	5	7	6.4 (5.1)	7.6 (10.1)
3	4	7	6.6 (5.3)	7.2 (9.7)

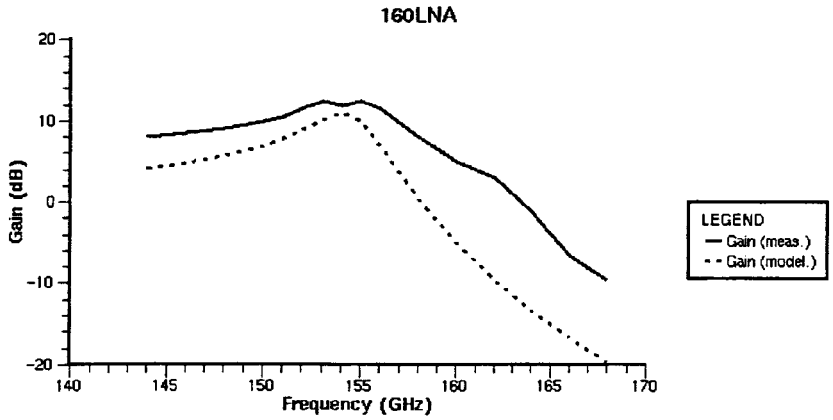


Fig. 9. The simulated and measured small-signal gain versus frequency (model: $V_d = 0.9$ V, $I_{\rm ds} = 8$ mA, measurement: $V_d = 1.4$ V, $I_{\rm ds} = 10$ mA).

compression effect was also roughly investigated under three input power levels. Table I lists the output power and gain at three input power levels under identical bias conditions at 155 GHz. As can be observed, the power gain of the amplifier was compressed by about 1.5 dB when the input power was increased from -18.75 to -8.75 dBm.

The spot noise temperature of the amplifier was measured with a calibrated-noise test system normally used to measure waveguide mixers. A block diagram appears in Fig. 8. The system was calibrated using room-temperature and liquid-nitrogen loads at the input horn of a subharmonically pumped planar-Schottky-diode mixer with a double-sideband noise temperature between 2000 K and 3000 K. The IF test system is precalibrated to read noise power in degrees using room temperature and 77-K coaxial loads. The reference plane for the test set is the end of the IF cable, which attaches to the output port of the mixer. During measurements, the mixer noise and conversion loss (reference noise temperature in Fig. 8) are determined by placing the hot and cold black-body loads at the input of the WR5 horn attached to the mixer input RF port. The horn is then moved to the output port of the amplifier and the measurement is repeated. Ignoring amplifier output mismatch, the gain and noise of the amplifier is simply given by

$$G_{\rm amp}({\rm dB}) = L_{\rm mixer} + L_{\rm mixer+amp}$$
$$T_{\rm amp} = T_{\rm mixer+amp} - T_{\rm mixer}/G_{\rm amp}.$$

The amplifier NF is then

$$\mathrm{NF(dB)} = 10\log(T_{\rm amp}/290 + 1).$$

The amplifier was then inserted between the mixer and horn and the deembedded loss (now gain) and excess-input noise temperature were backed out of the measured response. No correction for amplifier-to-mixer mismatch was made. The gain and noise were measured at three representative frequencies: 150, 155, and 160 GHz. The output intermediate frequency was fixed at 1.5 GHz and the predetection bandwidth for the spot noise measurement was 10 MHz. The results, accounting for 2.5-dB of transition loss under a drain voltage of 1.4 V with each stage drawing 10-mA current are listed in Table II. An NF of 6.8 dB with associated small-signal gain of 11 dB was measured at 155 GHz. Two amplifiers were measured, with one of the chips having approximately 1 dB lower NF than the other. Optimum bias conditions for minimum noise turned out to be 1.4-V drain bias for all three stages with 3, 5, and 7 mA of current for stages 1, 2, and 3, respectively. Under these conditions, from flange to flange, 6.4-dB NF (964 K) with 7.6-dB associated gain (NF of 5.1 dB, and 10.1-dB gain at the chip assuming 1.25-dB loss per transition) is obtained, as shown in Table III.

Fig. 9 is a plot of the simulated and measured small-signal gain from 144 to 168 GHz on the same graph. As compared with the simulated results, both the measured small-signal gain and NF agree to the data reasonably well below the peak gain

frequency 155 GHz. However, the simulated gain decreases faster than the measured one above 155 GHz, and the NF increases rapidly in simulation at 160 GHz. It is also noted that the data presented in this paragraph were taken at the drain bias of 1.4 V, while the models were derived via the HEMT device S- and noise-parameters under 0.9-V drain voltage with a fixed drain current of 8 mA. Some difference in small-signal gain was expected (0.5–1 dB per stage).

VI. Summary

We have described the design, structure, and measurements of a 155-GHz monolithic LNA using 0.1-μm PM InGaAs/InAlAs/InP HEMT technology. The three-stage single-ended 155-GHz monolithic LNA exhibits a small-signal gain of 12 dB at 155 GHz, and more than 10 dB of gain from 151 to 156 GHz. An NF of 5.1 dB with 10.1 dB associated is also achieved under a low current bias condition at 155 GHz. To the best of our knowledge, this is the highest frequency amplifier ever reported using three terminal devices. This is also the best reported performance for an amplifier at this frequency and the first measurements of amplifier noise above 140 GHz.

Acknowledgment

The authors would like to thank Y. H. Chung for the HEMT device modeling effort, T. Duong and T. Trinh for layout support, W. Jones, R. Dia, A. Freudenthal, and L. Go for the MMIC process, T. Block and D. Streit for the MBE effort, P. H. Liu for the E-beam lithography, B. Brunner for transition and chip assembly and fixture construction, and D. Tran and N. Nguyen for backside processing.

References

[1] K. H. G. Duh *et al.*, "A super low-noise 0.1 μm T-gate InAlAs-InGaAs-InP HEMT," *IEEE Microwave Guided Wave Lett.*, vol. 1, pp. 114–116, May 1991.

[2] K. L. Tan *et al.*, "140 GHz 0.1-μm gate-length pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.60}Ga_{0.40}As$/InP HEMT," in *IEEE Int. Electron. Device Meeting Dig.*, Washington D.C., Dec. 1991, pp. 239–242.

[3] K. L. Tan *et al.*, "94 GHz 0.1 μm T-gate low noise pseudomorphic InGaAs HEMT's," *IEEE Electron Device Lett.*, vol. 11, pp. 585–587, Dec. 1990.

[4] H. Wang, T. N. Ton, K. L. Tan, D. Garske, G. S. Dow, J. Berenz, M. W. Pospieszalski, and S. K. Pan, "110–120 GHz monolithic low noise amplifiers," *IEEE J. Solid-State Circuits*, vol. 28, pp. 988–993, Oct. 1993.

[5] R. Lai, H. Wang, K. L. Tan, G. I. Ng, D. C. Streit, P. H. Liu, J. Velebir Jr., S. Chen, J. Berenz, and M. W. Pospieszalski, "A monolithically integrated 120 GHz InGaAs/InAlAs/InP HEMT amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 4, pp. 194–195, June 1994.

[6] H. Wang, R. Lai, D. C. W. Lo, D. C. Streit, P. H. Liu, R. M. Dia, M. W. Pospieszalski, and J. Berenz, "A 140-GHz monolithic low noise amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 150–152, May 1995.

[7] M. V. Aust, T. W. Huang, M. Dufault, H. Wang, D. C. W. Lo, R. Lai, M. Biedenbender, and C. C. Yang, "Ultra low noise Q-band monolithic amplifiers using InP- and GaAs-based 0.1-μm HEMT technologies," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symp. Dig.*, San Francisco, CA, June 1996.

[8] H. Wang, R. Lai, S. Chen, and J. Berenz, "A monolithic 75–110 GHz balanced InP-based HEMT amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 3, pp. 381–383, Oct. 1993.

[9] T. Gaier, M. Seiffert, P. Meinhold, P. Lubin, M. Sholley, R. Lai, H. Wang, B. Allen, B. Osgood, T. Block, P. H. Liu, C. Jackson, and C. R. Lawrence, "Noise performance of a cryogenically cooled 94 GHz InP MMIC amplifier and radiometer," in *Int. Conf. Millimeter Submillimeter Waves Applicat. III Proc.*, vol. 2842, Denver, CO, Aug. 1996, pp. 588–593.

[10] H. Wang, G. S. Dow, B. Allen, T. N. Ton, K. Tan, K. W. Chang, T. H. Chen, J. Berenz, T. S. Lin, P. Liu, D. Streit, S. Bui, J. J. Raggio, and P. D. Chow, "High performance W-band monolithic InGaAs pseudomorphic HEMT LNA's and design/analysis methodology," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 417–428, Mar. 1992.

[11] H. Wang, G. I. Ng, R. Lai, Y. Hwang, D. C. W. Lo, R. Dia, A. Freudenthal, and T. Block, "Fully passivated W-band InAlAs/InGaAs/InP monolithic low noise amplifiers," *Proc. Inst. Elect. Eng.*, vol. 143, no. 5, pp. 361–366, Oct. 1996.

[12] P. M. Smith, "Status of InP HEMT technology for microwave receiver applications," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 2328–2333, Dec. 1996.

[13] Y.-C. Shih, T.-N. Ton, and L. Q. Bui, "Waveguide-to-microstrip transitions for millimeter-wave applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, New York, NY, June 1988, pp. 473–475.

Huei Wang (S'83, M'87, SM'95) was born in Tainan, Taiwan, R.O.C., on March 9, 1958. He received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Michigan State University, East Lansing, in 1984 and 1987, respectively.

During his graduate study, he was engaged in research on theoretical and numerical analysis of EM radiation and scattering problems. He was also involved in the development of microwave remote detecting/sensing systems. In 1987, he joined the Electronic Systems and Technology Division, TRW, where he was a Member of technical staff and Staff Engineer responsible for MMIC modeling of computer-aided design (CAD) tools, MMIC testing evaluation, and design, and then became the Senior Section Manager of the MMW Sensor Product Section, RF Product Center. In 1993, he visited the Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C., to teach MMIC-related topics, and returned to TRW in 1994. He joined the faculty of the Department of Electrical Engineering, National Taiwan University, as a Professor in 1998.

Dr. Wang is a member of Phi Kappa Phi and Tau Beta Pi.

Richard Lai was born in Evanston, IL, in 1964. He received the B.S.E.E. degree from the University of Illinois at Urbana-Champaign in 1986, and the M.S.E.E. and Ph.D. degrees from the University of Michigan at Ann Arbor, in 1988 and 1991, respectively.

In 1991, he joined the Advanced Microelectronics Laboratory, TRW, as a Product Engineer, where he is involved in the research, development, and production of advanced GaAs- and InP-based HEMT device and MMIC technologies into various military and commercial MMW applications. Since 1994, he has been the Principal Investigator for an advanced HEMT research and development project at TRW, and is currently the Product Engineering Manager for HEMT MMIC products. He has authored and co-authored over 60 papers and conference presentations in the area of advanced GaAs and InP-based device and circuit technology.

Yon-Lin Kok received the B.S. degree in electrophysics from the National Chiao-Tung University, Tsin-Chu, Taiwan, R.O.C., in 1980, the M.S. degree in electrical engineering from Michigan State University, East Lansing, in 1983, and the Ph.D. degree from Purdue University, West Lafayette, IN, in 1988.

He was a Research Assistant at Michigan State and Purdue Universities, where he studied image synthesis, restoration, and diffractive optics. From September 1988 to August 1994, he was an Assistant Professor of electrical engineering at the University of South Alabama, Mobile. From September 1994 to June 1995, he was a Visiting Professor at the University of Delaware, Newark. His research interests include EM scattering, binary optics, and communication systems. In July 1995, he joined the TRW RF Product Center, Redondo Beach, CA, where his work has focused on the design and testing of MMIC's and subsystems based on submicron GaAs and InP HEMT/heterojunction bipolar transistor (HBT) technologies.

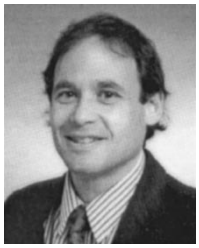
Tian-Wei Huang received the B.S. degree in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, R.O.C., in 1987, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles, in 1990 and 1993, respectively.

In 1993, he joined the RF Product Center, TRW, Redondo Beach, CA, where his work has been focused on the design and testing of MMIC's using GaAs- and InP-based HEMT technology. In 1998, he joined the Wireless Broadband Network Division, Lucent Technologies, Milpitas, CA, where he has been involved in the design of MMW wireless telecommunication systems.

Michael V. Aust, photograph and biography not available at the time of publication.

Yaochung C. Chen (M'92) was born in Taiwan, R.O.C., in 1959. He received the B.S.E.E. degree from the National Chiao-Tung University, Tsin-Chu, Taiwan, R.O.C., in 1982, the M.B.A. degree from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1984, and the M.S.E. and Ph.D. degrees from the University of Michigan at Ann Arbor, in 1990 and 1992, respectively, all in electrical engineering. His Ph.D. research concentrated on MBE and characterization of GaAs- and InP-based PM heterostructures and devices.

From 1992 to 1994, he was an Assistant Research Scientist at the University of Michigan, where he conducted research in MBE of strained materials and fabrication and characterization of PM HEMT's and HBT's. In May 1994, he joined Hughes Aircraft Company, where he participated in the development of manufacturing technologies of pseudomorphic HEMT's and HBT's and was responsible for the process development, device characterization, and physical modeling of GaAs PM HEMT's for high-power and high-efficiency applications. He is currently with the Space and Electronics Group, TRW, Redondo Beach, CA, where he is responsible for the development of InP-based HEMT's for MMW high-power and high-efficiency amplifiers. His research interests cover device physics, fabrication process, and MMIC design.

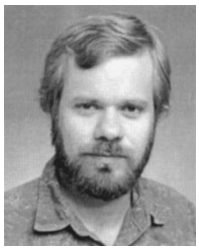


Peter H. Siegel (S'77–M'83–SM'98) was born in New Rochelle, NY, in August 1954. He completed his undergraduate work at Colgate University, Hamilton, NY, in 1976, and received the M.S. and Ph.D. degrees in electrical engineering from Columbia University, New York, NY, in 1978 and 1983 respectively.

In 1975, he was with the NASA Goddard Space Flight Center, Institute for Space Studies, New York, NY, where he worked on MMW mixers and multipliers. In 1984, he moved to the Central Development Laboratory, National Radio Astronomy Observatory, where he spent three years working on the millimeter receivers for the NRAO Kitt Peak 12 meter telescope. In 1989, he joined the Advanced Devices Group, California Institute of Technology, Jet Propulsion Laboratory (JPL), Pasadena. In 1994, he formed and became Supervisor of the JPL Submillimeter Wave Advanced Technology (SWAT) team, which is currently composed of approximately 20 engineers and scientists, who provide technology development and instrumentation support for NASA's advanced millimeter and submillimeter-wave missions. His research interests include millimeter- and submillimeter-wave devices, components, and subsystems.

Todd Gaier received the Ph.D. degree in physics from the University of California at Santa Barbara, in 1993.

He is currently a Senior Member of the Technical Staff at the Jet Propulsion Laboratory, Pasadena, CA, where he has worked on a variety of MMW instruments using HEMT amplifiers, including receivers for radio astronomy at 15, 23, 30, 44, and 94 GHz. He is the Technical Lead on the technology for a program to develop MMIC-based receivers for Earth remote-sensing applications up to 210 GHz.



Robert J. Dengler was born in Whittier, CA, in July 1963. He received the B.S. degree in electrical and computer engineering from the California State Polytechnic University, Pomona, in 1989.

He is currently a Member of the engineering staff at the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, where he is primarily involved with the development of test instrumentation for, and design, construction, and testing of submillimeter receivers and components for spaceborne applications.

Barry R. Allen (S'83–M'83) was born in Cadiz, KY. He received the S.B. degree in physics and the S.M. and Sc.D. degrees in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, in 1976, 1979, and 1984 respectively.

From 1970 to 1975, he was with the Chesapeake and Potomac Telephone Company of Virginia, where he supported microwave and radio telecommunications systems. From 1975 to 1983, he was a Member of the Research Laboratory of Electronics, MIT, where he was responsible for the development of room-temperature and cryogenic low-noise radio-astronomy receiving systems from 300 MHz to 43 GHz. In 1983, he joined TRW, Redondo Beach, CA, as a Senior Staff Member and has held a number of positions since then in both R&D and program management. Since 1983, he has been involved in all aspects of MMIC design and modeling. He is currently a Senior Scientist in the Electronics and Technology Division. He has authored or co-authored several papers on circuit applications of heterostructure devices and MMIC's. His main interests are low-noise receiving systems, MMW circuits, and accurate circuit modeling.

Dr. Allen became a TRW Technical Fellow in 1991. In 1992 and 1993, he was awarded the TRW Chairman's Award for Innovation for contributions to the application and manufacturing of GaAs MMIC's.